Claim(s)

What is claimed is:

1. An interconnect system for providing a signal path from a first circuit node of an integrated circuit (IC) to a second circuit node external to the IC, the IC being formed on a semiconductor substrate having horizontal upper and lower surfaces and having a peripheral edge extending between the upper and lower surfaces, the interconnect system comprising:

a conductor external to the semiconductor substrate extending downward proximate to the peripheral edge of the substrate from the upper surface to the lower surface,

first means for conductively linking the conductor to the first circuit node, and

second means for conductively linking the conductor to the second circuit node.

2. The interconnect system in accordance with claim 1 wherein the first means comprises:

a first conductive pad formed on the upper surface of the substrate and conductively linked to the first circuit node, and

means for conductively linking the first conductive pad to the conductor.

3. The interconnect system in accordance with claim 1 wherein the second means comprises:

a second conductive pad formed on the lower surface of the substrate and conductively linked to the conductor, and

third means for conductively linking the second conductive pad to the second circuit node.

4. The interconnect system in accordance with claim 3 wherein the conductor is attached to the peripheral edge of the substrate.

5. The interconnect system in accordance with claim 4 wherein said third means comprises solder conductively linking the second conductive pad to the second circuit node.

6. The interconnect system in accordance with claim 5 further comprising a first conductive pad formed on the upper surface of the substrate and conductively linked to the first circuit node, and

means for conductively linking the first conductive pad to the conductor.

7. The interconnect system in accordance with claim 1 wherein the first means comprises a first conductive pad formed on the upper surface of the substrate and conductively linked to the first circuit node, and means for conductively linking the first conductive pad to the conductor;

wherein the second means comprises a second conductive pad formed on the lower surface of the substrate and conductively linked to the conductor, and solder conductively linking the second conductive pad to the second circuit node; and

wherein the conductor is attached to the peripheral edge of the substrate.

8. The interconnect system in accordance with claim 1 wherein the conductor includes a portion extending horizontally under and proximate to the lower surface of the substrate.

9. The interconnect system in accordance with claim 8 wherein the conductor portion extending horizontally under and proximate to the lower surface of the substrate is attached to the lower surface of the substrate.

10. The interconnect system in accordance with claim 8 wherein the portion of the conductor extending horizontally under and proximate to the lower surface of the substrate

comprises resilient material and is spaced from the lower surface of the substrate.

11. The interconnect system in accordance with claim 10 wherein the second means comprises a conductive bump residing on and extending downward from the portion of the conductor extending horizontally under the lower surface of the substrate.

12. The interconnect system in accordance with claim 1 wherein the conductor includes a resilient portion extending under and spaced from the lower surface of the substrate, and

wherein the second means comprises a conductive bump for contacting the external circuit node, the bump residing on and extending downward from the resilient portion of the conductor extending under the substrate.

13. A method for fabricating an interconnect system for providing a signal path to a first circuit node of an integrated circuit (IC) contained on a portion of a semiconductor wafer having horizontal upper and lower surfaces, the method comprising the steps of:

a. forming a hole extending vertically through an area of the wafer adjacent to the IC, and

b. placing conductive material in the hole, the conductive material vertically extending through the hole, and

c. conductively linking the conductive material to the first circuit node.

14. The method in accordance with claim 13 further comprising the step of:

d. cutting on the wafer vertically along a horizontal saw-line extending across the hole such that the portion of the semiconductor wafer containing the IC includes a peripheral edge formed along the saw-line upon which a portion of the conductive material placed in the hole remains attached.

15. The method in accordance with claim 14 further comprising the step of:

e. forming a bond pad on the lower surface of the semiconductor wafer conductively linked to the conductor.

16. The method in accordance with claim 14 wherein the conductive material placed on the wafer at step b also extends from the hole horizontally along and attached to the lower surface of the semiconductor wafer under the portion of the semiconductor wafer containing the IC.

17. The method in accordance with claim 14 wherein the conductive material placed on the wafer at step b also extends from the hole horizontally along the upper surface of the semiconductor wafer on the portion of the semiconductor wafer containing the IC.

18. The method in accordance with claim 17 wherein the conductive material placed on the wafer at step b also extends from the hole horizontally along the lower surface of the semiconductor wafer on the portion of the semiconductor wafer containing the IC.

19. The method in accordance with claim 16 further comprising the steps of:

e. coating a portion of the conductive material extending along and attached to the lower surface of the portion of the semiconductor wafer containing the IC with resilient material, and

f. detaching the portion of the conductive material coated with resilient material from the lower surface of the portion of the semiconductor wafer containing the IC so that it forms a spring contact linked by the conductive material to the first circuit node.

20. A method for fabricating an interconnect system for providing a signal path to a first circuit node of an integrated circuit (IC) contained on a portion of a

semiconductor wafer having horizontal upper and lower surfaces, the method comprising the steps of:

a. forming a hole having an inner surface extending vertically through an area of the wafer adjacent to the IC,

b. placing a first layer of material on the lower surface of the wafer and on the inner surface of the hole; and

c. placing a second layer of conductive material over the first layer, the second layer being conductively linked to the first circuit node.

21. The method in accordance with claim 20 further comprising the step of:

d. placing a third layer of resilient conductive material over the second layer.

22. The method in accordance with claim 21 further comprising the step of:

e. cutting on the wafer vertically along a horizontal saw-line extending across the hole such that the portion of the semiconductor wafer containing the IC includes a peripheral edge formed along the saw-line, and wherein a portion of the first, second and third layers remains attached to the peripheral edge.

23. The method in accordance with claim 22 further comprising the step of:

f. removing a first portion of the first layer from between the second layer and the lower surface of the portion of the semiconductor wafer containing the IC.

24. The method in accordance with claim 23 further comprising the step of:

g. removing a second portion of the first layer from between the second layer and the peripheral edge of the portion of the semiconductor containing the IC.

25. The method in accordance with claim 20 wherein a portion of the first layer formed on the lower surface of the portion of the semiconductor waver includes a downward-projecting bump.

26. A method for interconnecting a first node of a first integrated circuit (IC) chip to a second node of a second IC chip, wherein the first IC chip has a first upper surface, a first lower surface and a peripheral edge extending between the first upper surface and the first lower surface, and wherein the second IC chip has a second upper surface, the method comprising the steps of:

a. providing a first conductive pad on the first lower surface of the first IC chip,

b. providing a second conductive pad on the upper surface of the second IC chip conductively linked to the second node,

c. forming a conductor on the peripheral edge of the first IC chip extending between the first upper surface and the first lower surface,

d. conductively linking the conductor to the first node and to the first conductive pad, and

e. conductively linking the first conductive pad to the second conductive pad.

27. The method in accordance with claim 26 wherein step e comprises the substeps of:

e1. placing solder on one of said first and second pads, and

e2. positioning the first IC chip over the second IC chip such that the solder contacts the first conductive pad and the second conductive pad.

28. A method for interconnecting a first node of a first integrated circuit (IC) chip to a second node of a second IC chip, wherein the first IC chip has a first upper surface, a first lower surface and a peripheral edge extending between the first upper surface and the first lower

surface, and wherein the second IC chip has a second upper surface, the method comprising the steps of:

a. providing a spring contact attached to the first IC chip, the spring contact including a conductive path linked to the first node, wherein the conductive path includes a first portion extending downward adjacent to the peripheral edge of the IC chip and includes a second portion extending in a substantially horizontal direction at an elevation below the first lower surface of the first IC chip;

b. providing a conductive pad on the second upper surface of the second IC chip conductively linked to the second node, and

c. conductively linking the second portion of the conductive path spring contact to the conductive pad on the upper surface of the second IC chip.

29. The method in accordance with claim 28 wherein the second portion of the conductive path extends under the first lower surface of the first IC chip.

30. The method in accordance with claim 28 wherein the second portion of the conductive path includes a downward-projecting conductive bump and wherein step c comprises positioning the first IC chip over the second IC chip such that the conductive bump contacts the conductive pad on the second upper surface of the second IC chip.

31. The method in accordance with claim 28 wherein the conductive path includes a first layer of conductive material and a second layer of resilient conductive material formed on the first layer.

32. The method in accordance with claim 28 wherein the second portion of the conductive path extends under the first lower surface of the first IC chip,

wherein the second portion of the conductive path includes a downward-projecting conductive bump and wherein step c comprises positioning the first IC chip over the

second IC chip such that the conductive bump contacts the conductive pad on the second upper surface of the second IC chip, and

wherein the conductive path includes a first layer of conductive material and a second layer of resilient conductive material formed on the first layer.

add A2